

We Claim:

1. A method for fabricating a vertical transistor, which comprises the steps of:

providing a monocrystalline semiconductor substrate having at least one trench formed therein with a lower section and an upper section, at least the lower section of the trench being lined with a storage dielectric and filled with at least one conductive material;

forming an auxiliary insulation layer on the conductive material;

depositing an epitaxial semiconductor layer on uncovered sidewalls of the upper section of the trench;

removing the auxiliary insulation layer;

conformally depositing a nitride layer, the nitride layer being so thin that it only partially impairs a current flow;

filling the trench with a doped further conductive material for producing an electrical connection between the conductive material situated in the lower section and a lower partial section of the epitaxial semiconductor layer, the lower partial section of the epitaxial semiconductor layer being

doped by indiffusion of dopants from the further conductive material to form a first doping region;

forming a gate dielectric on uncovered regions of the epitaxial semiconductor layer;

forming a gate electrode on the gate dielectric; and

forming a second doping region in an upper partial section of the epitaxial semiconductor layer.

2. The method according to claim 1, which further comprises:

forming an insulation collar in the trench and the insulation collar, proceeding from a transition region between the lower and upper sections, extends in a direction of the upper section; and

after the forming of the auxiliary insulation layer and before the depositing of the epitaxial semiconductor layer step, etching back the insulation collar as far as a plane lying above the auxiliary insulation layer, thereby uncovering the sidewalls of the trench above the insulation collar for the deposition of the epitaxial semiconductor layer.

3. The method according to claim 2, which further comprises

before the insulation collar is etched back, applying an further auxiliary layer to the auxiliary insulation layer.

4. The method according to claim 2, which further comprises forming the storage dielectric with an upper edge, and the upper edge, as a result of the etching-back, terminates approximately with an upper edge of the insulation collar.

5. The method according to claim 1, which further comprises forming the nitride layer to be thinner than 1 nm.

6. The method according to claim 5, which further comprises forming the nitride layer to have a thickness of about 4 - 8 Å.

7. The method according to claim 1, which further comprises forming the nitride layer to isolate the further conductive material from the epitaxial semiconductor layer.

8. The method according to claim 2, which further comprises before the gate electrode is formed, applying a further insulation layer to the further conductive material.

9. The method according to claim 2, which further comprises:

forming the conductive material to contain a material forming an inner electrode of a trench capacitor and a conductive connecting material, which covers the inner electrode and is surrounded by the insulation collar.

10. The method according to claim 1, which further comprises forming the further conductive material from doped polysilicon.

11. A semiconductor memory cell, comprising:

a monocrystalline semiconductor substrate having a trench formed therein with an upper section, a lower section, and sidewalls;

a trench capacitor disposed in said lower section, said trench capacitor having an inner electrode formed from a conductive material;

an epitaxial semiconductor layer disposed on said sidewalls of said upper section of said trench and having a lower partial section, an upper partial section, and a lower edge;

a vertical transistor disposed in said upper section of said trench and formed completely in said epitaxial semiconductor layer, said vertical transistor having a first doping region

formed in said lower partial section of said epitaxial semiconductor layer and a second doping region formed in said upper partial section;

a storage dielectric lining said sidewalls of said lower section and having an upper edge, said lower edge of said epitaxial semiconductor layer extending at least as far as said upper edge of said storage dielectric;

an insulation collar disposed in a transition region between said lower section and said upper section, said insulation collar covering said storage dielectric;

a further conductive material electrically connecting said inner electrode of said trench capacitor to said first doping region of said vertical transistor; and

a nitride layer disposed at least between said further conductive material and said epitaxial semiconductor layer, said nitride layer having a thickness dimensioned to only partially impair a current flow.

12. The semiconductor memory cell according to claim 11, further comprising a conductive connecting material covering said inner electrode, surrounded by said insulation collar, and covered by said further conductive material.

13. The semiconductor memory cell according to claim 12, wherein said nitride layer is further disposed between said conductive connecting material and said further conductive material.

14. The semiconductor memory cell according to claim 11, wherein said nitride layer is thinner than 1 nm.

15. The semiconductor memory cell according to claim 14, wherein said nitride layer has a thickness of about 4 - 8 Å.

16. The semiconductor memory cell according to claim 12, wherein said conductive material of said inner electrode, said conductive connecting material and said further conductive material are all doped polysilicon.

17. The semiconductor memory cell according to claim 11, wherein said vertical transistor has a gate electrode; and further comprising an insulation layer disposed between said further conductive material and said gate electrode.

18. The semiconductor memory cell according to claim 11, wherein said epitaxial semiconductor layer extends beyond an

upper edge of said insulation collar in a direction of said lower section of said trench.

19. The semiconductor memory cell according to claim 18, wherein said epitaxial semiconductor layer extends beyond said upper edge of said insulation collar by about 30 nm.

20. The semiconductor memory cell according to claim 11, wherein said epitaxial semiconductor layer extends beyond an upper edge of said storage dielectric in a direction of said lower section of said trench.

21. The semiconductor memory cell according to claim 20, wherein said epitaxial semiconductor layer extends beyond said upper edge of said storage dielectric by about 30 nm.